Listing of Claims

The following listing of claims replaces all prior versions.

1. (Currently amended) An integrated circuit comprising:

a plurality of serializer/deserializers (SERDESs);

core processing logic integrated with each of said plurality of SERDESs and connected to each of said plurality of SERDESs to exchange signals therewith; and

a plurality of functionally identical testers integrated with said plurality of SERDESs and said core processing logic, said testers being connected to individually test each of said plurality of SERDESs, each of said testers being enabled to detect performance characteristics of an individual one of said plurality of SERDESs independently of other said testers and concurrently with said plurality of SERDESs, wherein a bit error rate for each of said plurality of SERDESs is individually identified, and wherein said testers perform loop-back testing, static data testing and dynamic data testing;

wherein each of said testers is connected to a common test bus that is integrated with said plurality of SERDESs and said testers, said common test bus being separate from a data bus, each of said testers having a unique address that enables independent accessibility of each of said testers via said test bus, said test bus being dedicated to providing signaling for said enablement to detect performance characteristics of said individual one of said plurality of ~~individual~~ SERDESs and further comprising a built in self-test (BIST) state machine integrated with said plurality of SERDESs and said testers, said BIST being connected to said test bus and being configured to sequence test operations by each of said ~~individual said~~ testers.

2. (Currently amended) The integrated circuit of claim 1 further comprising a semiconductor substrate on which said plurality of SERDESs, said core processing logic and said testers are fabricated.

3. (Currently amended) The integrated circuit of claim 1 wherein each of said testers includes a test controller and a test interface, each of said testers being dedicated to ~~a specific~~ said individual one of said plurality of SERDESs, said test interface of each of said testers being

coupled between said core processing logic and said SERDES to which said each of said testers is dedicated, said tester controller being configured to select among a normal operation mode and a plurality of test modes for operation of said test interface.

4. (Currently amended) The integrated circuit of claim 3 wherein ~~each~~ said test interface includes a test pattern generator that is connected to inputs of parallel data of each of said plurality of SERDESs to which said test interface is dedicated, said test interface further including an error detector connected to outputs of parallel data from each of said plurality of SERDESs.

5. (Canceled)

6. (Currently amended) The integrated circuit of claim 1 further comprising an input/output tester controller integrated with said plurality of SERDESs and said testers, said input/output tester controller being coupled between said test bus and an output of said integrated circuit for signal communication with an external source for sequencing test operations.

7. (Canceled)

8. (Currently amended) The integrated circuit of claim 1 wherein said testers are responsive to individual commands and are configured to be individually but concurrently operated, said testers having a one-to-one correspondence with said plurality of SERDESs.

9. (Currently amended) An integrated circuit comprising:

a single semiconductor substrate onto which integrated circuitry is fabricated;

core circuitry integrated onto said substrate;

a plurality of SERDESs integrated onto said substrate, each of said plurality of SERDESs having parallel data inputs and parallel data outputs and having serial data inputs and outputs;

a plurality of functional test interfaces (FTIs) integrally formed with said substrate, each of said FTIs being uniquely associated with a one of said SERDESs and being

connected to said parallel data inputs and outputs of said associated one of said SERDESs, each of said FTIs being enabled to individually and concurrently test performances of each of said plurality of SERDESs wherein a bit error rate for each of said plurality of SERDESs is individually identified, and wherein said FTIs perform loop-back testing, static data testing and dynamic data testing;

a plurality of functional test controllers (FTCs) integrally formed with said substrate, each of said FTCs being uniquely associated with a one of said FTIs and being configured to select among operational modes of said associated one of said FTIs; and

an input/output controller (IOC) and common test bus integrally formed with said substrate, said common test bus being dedicated to providing signaling for enablement of testing, said common test bus being separate from a data bus, said IOC being connected to each of said FTCs via said common test bus to transmit individually addressed commands to each of said FTCs, said IOC further being connected to exchange signals with an external device.

10. (Currently amended) The integrated circuit of claim 9 wherein each of said FTIs is configured to operate in a plurality of alternative said operational modes, including a normal-operation mode in which data is transmitted between said core circuitry and said associated one of said SERDESs via each of said FTIs.

11. (Currently amended) The integrated circuit of claim 9 wherein each of said FTIs includes a pattern generator connected to said parallel data inputs of said associated one of said SERDESs and includes an error detector connected to said parallel data outputs of said associated one of said SERDESs.

12. (Original) The integrated circuit of claim 9 further comprising a built-in-self-tester (BIST) integrally formed on said substrate, said BIST being connected and configured to activate testing via said FTIs.

13. (Original) The integrated circuit of claim 9 wherein each of said FTIs is connected to said IOC via a common test bus, said FTIs also being connected to said core circuitry.

14. (Currently amended) The integrated circuit of claim 13 wherein each of said FTIs is assigned a unique address, said IOC being enabled to individually manipulate each of said FTIs by employing said unique addresses.

15. (Currently amended) A method of testing operations of serializer/deserializers (SERDESs) of an integrated circuit comprising the steps of:

embedding a plurality of test interfaces within said integrated circuit such that each of said test interfaces is specific to a one of said SERDESs with respect to exchanging parallel data, including forming each of said test interfaces to include a test pattern generator connected to parallel data inputs of said SERDESs to which each of said test interfaces is specific and further including forming each of said test interfaces to include an error detector to receive parallel data from said SERDESs to which said test interface is specific, wherein each of said ~~a plurality of~~ SERDESs is individually and concurrently tested and a bit error rate of each of said SERDESs is individually identified, and wherein said testers perform loop-back testing, static data testing and dynamic data testing;

embedding test controllers within said integrated circuit such that each of said test controllers is specific to a one of said test interfaces with respect to triggering test operations by said one of said test interfaces;

providing an integrated circuit output that enables said test controllers to be individually addressed; and

embedding an input/output controller (IOC) and a test bus within said integrated circuit, including connecting said IOC between said integrated circuit output and said test bus and including linking each said test controller to said test bus, said test bus being separate from a data bus.

16. (Canceled)

17. (Original) The method of claim 15 further comprising a step of concurrently enabling all of said test interfaces to simultaneously monitor performances of said SERDESs.

18. (Currently amended) The method of claim 15 further comprising the step of embedding a built-in-self-test (BIST) state machine within said integrated circuit such that said BIST is connected to each of said test controllers.

19. (Original) The method of claim 15 further comprising the step of forming an insulative package to house circuitry of said integrated circuit.

20. (Canceled)